REMARKS

Claims 1-14 and 57-73 remain in the present application. Applicant respectfully requests further examination and reconsideration of the rejections based on the amendments and arguments set forth below.

Allowable Subject Matter

Applicant would like to thank the Examiner for the indication that Claims 3-14, 65-66 and 72-73 would be allowable if rewritten in independent form including all of the limitations of any base claims and any intervening claims.

Claim Rejections – 35 U.S.C. §102

Claims 1-2, 57-64 and 67-71 are rejected in the present Office Action under 35 U.S.C. §102(e) as being anticipated by United States Patent Number 6,678,834 to Aihara et al. (hereafter referred to as "Aihara"). Applicant has reviewed the cited reference and respectfully submits that the embodiments of the present invention as recited in Claims 1-2, 57-64 and 67-71 are neither anticipated nor rendered obvious by Aihara for the following reasons.

Applicant respectfully directs the Examiner to independent Claim 1, which recites a data processing pipeline comprising (emphasis added):

> a first circuit for classifying a received data set, wherein the first circuit is operable to select a process mode for processing the received data set to reduce power consumption without significantly sacrificing quality and performance, and wherein the process mode is selected based upon a classification of the received data set; and
>
> a second circuit coupled to the first circuit, wherein the second circuit is operable to process data received from the first circuit, and wherein processing is performed in accordance with the process mode selected by the first circuit.

Independent Claims 57 and 58 recite limitations similar to independent Claim 1. Claims 2-7 depend from independent Claim 1 and recite further limitations to the claimed invention.

Applicant respectfully submits that Aihara fails to teach or suggest the limitations of "wherein the first circuit is operable to select a process mode for processing the received data set" as recited in independent Claim 1. As recited and described in the present application, a first circuit is operable to select a process mode for processing a received data set.

In contrast to the claimed embodiments, Applicant understands Aihara to teach the selection of a video clock (Vclk) for an LCD display. For example, as shown in Figures 3 and 5 of Aihara, a Vclk is sent by video controller 7 to LCD panel 27 for use in displaying images on LCD panel 27 (col. 7, lines 62-65; col. 8, lines 63-66). More specifically, Aihara teaches that "[t]he output of the LCD output circuit 17 is performed at the speed of the Vclk" (col. 8, lines 64-66). As such, Aihara teaches away from the claimed embodiments by teaching that a *video clock* is selected for *outputting and displaying* data instead of selection of a *process mode* for *processing* graphical data as claimed.

Applicant respectfully submits that Aihara fails to teach or suggest the limitations of "wherein processing is performed in accordance with the process mode selected by the first circuit" as recited in independent Claim 1. As recited and described in the present application, a second circuit is operable to process data in accordance with a process mode selected by a first circuit

In contrast to the claimed embodiments, Applicant understands Aihara to teach an LCD display which *displays* data in accordance with a *video clock signal* received from a video controller. For example, as shown in Figures 3 and 5 and as discussed above, Aihara teaches that Vclk is sent by video controller 7 to LCD panel 27 for use in displaying images on LCD panel 27 (col. 7, lines 62-65; col. 8, lines 63-66). Applicant respectfully submits that displaying in accordance with a video clock signal is very different from processing in accordance with a selected process mode as recited in independent Claim 1. As such, Applicant respectfully submits that Aihara teaches away from the claimed embodiments by teaching that an LCD display *displays* in accordance with a *video clock signal* instead of a circuit *processing* graphical data in accordance with a *selected process mode* as claimed.

For these reasons, Applicant respectfully submits that independent Claim 1 is neither anticipated nor rendered obvious by Aihara, thereby overcoming the 35 U.S.C. §102(e) rejection of record. Since independent Claims 57 and 67 recites limitations similar to those discussed above with respect to independent Claim 1, independent Claim 57 and 67 also overcomes the 35 U.S.C. §102(e) rejections of record. Since dependent Claims 2, 58-64 and 68-71 recite further limitations to the invention claimed in independent Claim 1, dependent Claims 2, 58-64 and 68-71 are also neither anticipated nor rendered obvious by Aihara. Therefore, Claims 1-2, 57-64 and 67-71 are allowable.

CONCLUSION

Applicant respectfully submits that Claims 1-14 and 57-73 are in condition for allowance and Applicant earnestly solicits such action from the Examiner.

The Examiner is urged to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,

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